REMARKS

By this amendment, claim 36 has been cancelled and claims 1, 34, and 35 have been amended. Accordingly, claims 1-35, 37, and 38 are pending in the present application. The claim amendments are new claims supported by the specification, the accompanying figures, and claims as originally filed, with no new matter being added. In particular, support for the amendments can be found at page 10, lines 6-21, page 11, lines 2-5 and 13-17 of the application as filed. Accordingly, favorable reconsideration of the pending claims is respectfully requested.

1. Rejection Under the Judicially Created Doctrine of Double Patenting

Claims 1-35 have been rejected under the judicially created doctrine of obviousness-type double patenting over claims 1-32 of U.S. Patent No. 6,107,183 to Sandhu et al. for the reasons set forth on pages 6 and 7 of the Office Action.

This rejection will be addressed when the Examiner indicates the allowable subject matter.

2. Rejections Under 35 U.S.C. §103

Claims 1-10 and 36 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,445,996 to Kodera et al. (hereinafter "*Kodera*") taken with U.S. Patent No. 5,708,303 to Jeng (hereinafter "*Jeng* '303"), U.S. Patent No. 5,486,493 to Jeng (hereinafter "*Jeng* '493"), and U.S. Patent No. 5,641,382 to Shih et al. (hereinafter "*Shih*") for the reasons set forth on pages 2-4 of the Office Action. Applicants respectfully traverse.

Initially, Applicants incorporate by reference their arguments presented in their responses to prior Office Actions in this matter. The following arguments are presented to supplement those prior arguments for the patentability of claims 1-10 and 36.

Applicants respectfully submit that the above rejection fails to give proper weight to a solution provided by the presently recited claims - the reduction of fringe capacitance. Claim 1 therefore now recites, *inter alia*, "the layer of dielectric material extending above the upper surface of the adjacent lines of conductive material and below the lower surface of the adjacent lines of conductive material sufficient to reduce the fringe capacitance therebetween, but not extending directly over or under the upper and lower surfaces of the adjacent lines of conductive material."

In contrast, Kodera does not teach a dielectric material layer extending below the bottom surface of a conductive layer, does not teach the use of low dielectric constant materials, does not address the problem of fringe capacitance, and in fact clearly illustrates a failure to comprehend, appreciate, or design for a solution to the problem of fringe capacitance. Rather, *Kodera* seeks to improve a polishing operation on the upper surface of the dielectric layers 217, 246. In particular, *Kodera* uses a carbon spacer film to create a polishing stop. Although this creates a final product with a dielectric layer that extends higher than the adjacent conductor layer, this is not done to address the problem of fringe capacitance.

Similarly, neither of *Jeng* '303 or *Jeng* '493 teach or suggest the claimed methods of addressing the problem of fringe capacitance. Although both references acknowledge the use of low dielectric constant dielectric materials, they do not teach or suggest extending a low dielectric constant dielectric layer above and below the upper and lower surfaces of adjacent conductive lines *to prevent fringe capacitance.*

Finally, *Shih* is cited for disclosing etching below the lower surface of adjacent conductive lines. Again, Applicants respectively assert that *Shih* in fact expressly teaches away from any motivation to do so:

> [T]he etching time used to form the electrode pattern 15 can be

> increased to remove the silicon nodules but this will result in over etched regions 18 of the dielectric layer 12 and deterioration of the photoresist pattern 16 used to form the electrode pattern. The deterioration of the photoresist pattern can cause loss of photoresist at the pattern edge 17 resulting in a less desirable electrode cross section profile.

Shih at column 1, lines 57-64. Thus, while *Shih* acknowledges that is known to inadvertently overetch adjacent to conductive lines as part of the process to remove silicon nodules, the practice is clearly discouraged because of its associated problems of overetched regions of dielectric layers and loss of photoresist at the pattern edge. Therefore, the expressly acknowledged deficiencies of overetching in *Shih* would prevent there being any motivation to modify *Kodera* by combining the teachings of *Kodera* and *Shih* to overetch silicon dioxide layer 202 in *Kodera.*

Claims 2-10 depend from claim 1, include the limitations therein, and are therefore patentable over the cited references for at least the reasons foregoing reasons presented hereinabove with respect to claims 1. Accordingly, Applicants submit that claims 1-10 are not obvious in view of *Kodera*, *Jeng* '303, *Jeng* '493 and *Shih* and Applicants therefore respectfully request that the rejection of claims 1-10 under 35 U.S.C. § 103(a) be withdrawn.

Claims 11-35, 37, and 38 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over *Kodera* in view of *Jeng* '303, and *Jeng* '493, and *Shih* for the reasons set forth on pages 5-7 of the Office Action. Applicants respectfully traverse.

Initially, Applicants incorporate by reference their arguments presented in their responses to prior Office Actions in this matter. The following arguments are presented to supplement those prior arguments and provide additional non-limiting bases for the patentability of claims 11-35, 37, and 38.

Claim 11 recites, *inter alia*:

patterning said conductive layer by:

forming a mask layer on said conductive layer; and

etching through said conductive layer and into said first dielectric layer, leaving a space between adjacent remaining portions of said conductive layer that extends below the lower surface of said conductive layer, said adjacent remaining portions of said conductive layer forming lines of conductive material each having an upper surface;

depositing an additional layer on the upper surfaces of lines of conductive material and on said first dielectric layer;

(emphasis added). Claim 22 recites, *inter alia*:

patterning said metal layer by:

forming a mask layer on said metal layer; and

etching through said metal layer and into said first dielectric layer, leaving a space between adjacent remaining portions of said metal layer that extends below the lower surface of said metal layer, said adjacent remaining portions of said metal layer forming metal lines each having an upper surface;

depositing a thin layer of silicon dioxide conformably over said metal lines and selectively on said upper surfaces of said metal lines;

(emphasis added). The results of these embodiments are in part depicted by Figures 5-7 of the present application and the accompanying text in the specification (pages 7-14), which show that these embodiments include first etching a conductive layer and then depositing an additional layer.

Kodera does not teach or suggest such methods. Rather, *Kodera* forms a polysilicon wiring film 203, forms a carbon film 244 over polysilicon wiring film 203, forms a photoresist layer 245 over carbon film 244, and then sequentially etches carbon layer 244 and polysilicon layer 203. This is a different method with steps occurring in a different order than the present claims recite.

Jeng '303, *Jeng* '493, and *Shih* do not address the formation of an additional layer as presently claimed and therefore cannot overcome the deficiencies of *Kodera* to teach or suggest the recited limitations.

Claims 12-21, 23-33, 37, and 38 depend from either claim 11 or claim 22, include the limitations therein, and are therefore patentable over the cited references for at least the reasons foregoing reasons presented hereinabove with respect to claims 11 and 22.

Additionally, claims 25-27 recite additional limitations not taught or suggested by the cited references. These include, for example: "etching said additional layer" (claim 25); "wherein said step of performing an etch on said additional layer etches the corner of the additional layer faster than the top surface of the additional layer" (claim 26); and "wherein said step of performing an etch on said additional layer etches in an argon or an argon-plus-fluorine based plasma (claim 27)." *See e.g.* Figure 6 of the present application.

Further, present claims 34 and 35 recite, *inter alia*: "wherein said second dielectric layer and said additional layer are formed of the same material." *Kodera* has no such teaching or suggestion. Rather, *Kodera* discloses only the use of carbon because "[s]ince a carbon layer is polished at a very low rate, the use of a carbon layer provides a large ratio of the rate of polishing the proper object to be polished to that of polishing the stopper." *Kodera* at column 14, lines 61-64.

None of *Jeng* '303, *Jeng* '493, or *Shih* can be combined with *Kodera* to overcome these deficiencies of *Kodera* because to do so would destroy the function of *Kodera*. The use of a dielectric material by *Kodera* as a stopper 244 could not function as the intended stopper because it would be removed too quickly, thus eliminating the entire purpose and intent of the teachings of *Kodera*. *See e.g. Kodera* at column 26, lines 20-37.

Finally, claim 35 has also been amended to recite, "etching through said additional layer and said conductive layer in a single etch step." Because *Kodera* uses a carbon film 244, separate etch steps are required, O_2 and CF_4. *Kodera* at column 31, lines 58-64. Therefore, *Kodera* cannot teach or suggest the limitations of present claim 35.

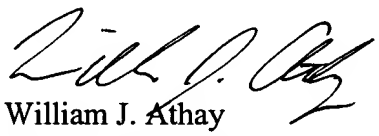
Accordingly, Applicants therefore respectfully assert that claims 11-35, 37, and 38 are patentable over the cited references and request that the rejection of the claims under 35 U.S.C. § 103(a) be withdrawn.

CONCLUSION

In view of the foregoing, Applicants respectfully request favorable reconsideration and allowance of the present claims. In the event the Examiner finds any remaining impediment to the prompt allowance of this application that could be clarified by a telephone interview, the Examiner is respectfully requested to contact the undersigned attorney.

Dated this 3rd day of February 2003.

Respectfully submitted,



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